REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons which follow.

Claim amendments

Claims 1 and 5 are currently being amended. Claims 1 and 5 are amended to put these claims in better form for U.S. Practice. Applicant submits that the amendments to claims 1 and 5 do not narrow these claims, and are not done in response to a rejection of the claims.

Claims 9 and 10 are being added.

This amendment adds, changes and/or deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, are presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 1-10 are now pending in this application.

Drawings

The drawings were objected to. Specifically, the Office Actions stated that "exposure light" in claim 1, line 7 and "the exposure step of radiating exposure light" in claim 5, line 8 must be shown in the drawings. Applicant submits that the Figures, which illustrate an optical section 36 that provides radiating exposure light, along with the accompanying text of the specification, provide sufficient supporting and enabling disclosure for claims 1 and 5. However, in the interest of expediting prosecution of the present application, applicant has amended Figure 1 to illustrate exposure light 50 provided by the optical section 36. The specification has been amended to be consistent with the amendment to Figure 1, namely to include the reference numeral 50.

Rejection under 35 U.S.C. § 102

Claims 1-8 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,489,966 to Kawashima et al. (hereafter "Kawashima"). Applicant respectfully traverses this rejection for at least the following reasons.

Independent claim 1 is directed to a wafer edge exposure apparatus for exposing an edge of a semiconductor wafer. The apparatus includes an optical section for irradiating exposure light toward the edge of the semiconductor wafer, and a sensor for detecting the height of the edge. On a basis of a value detected by the sensor, a focus position control mechanism controls the focal position of exposure light originating from the optical section. Thus, in the present invention as recited in claim 1, the sensor detects the height of the edge of the semiconductor wafer, and based on a value detected, the focal position of exposure light is controlled. The apparatus of claim 1 may solve problems associated with exposing the edge of resist films on a substrate and allows for appropriate exposure of an edge of the resist film formed over a substrate (see present specification, page 4, lines 14-22). Applicant submits that Kawashima fails to disclose or suggest a system where a sensor detects the height of the edge of the semiconductor wafer, and based on a value detected, the focal position of exposure light is controlled.

Kawashima discloses a projection exposure apparatus (see title). The Kawashima apparatus includes a reduction projection lens 8, an X-Y-Z stage 10 for supporting a wafer 9, and a reference flat mirror 17 having a mirror surface whose height is substantially the same as that of an upper surface of the wafer 9 (Fig. 1; col. 6, lines 7-18). The Kawashima apparatus also includes an off-axis surface position detecting system comprising a light projecting optical system 11 that concentrates light on the flat mirror 17, and a detection optical system 12 that receives reflected light from the flat mirror 17 (col. 6, lines 54-64). A signal indicative of the positional deviation of the flat mirror 17 as measured by the detection optical system 12 is transmitted to an autofocus control system 19, that supplies an instruction to move the stage 10 (col. 7, lines 8-14). For detection of the focus position, the autofocus control system 19 moves the reference mirror 17 up or down (col. 7, lines 14-20). For control of the wafer 9 at the time of exposure, the portion of the wafer to be exposed is placed at the position of the flat mirror (col. 7, lines 20-25).

Kawashima fails to disclose that surface position detection system includes a sensor that detects the height of the edge of the semiconductor wafer. Instead as described above, the Kawashima system detects the height of the surface of a reference flat mirror. The Kawashima system, which detects the height of a reference mirror instead of a height of semiconductor substrate directly, is thus quite different from the apparatus as recited in claim 1, and fails to anticipate claim 1.

Moreover, Kawashima is not concerned with detecting the height of an edge of a semiconductor wafer and adjusting the focus based on that detection, but instead is concerned with correcting for optical system defects due to factors such as temperature and pressure (see col. 10, lines 36-58). Kawashima does not suggest determining the height of a surface of a specific portion of a wafer, much less directly detecting that height as in claim 1, but instead indirectly estimates the height of a wafer surface on average through detecting the height of a surface of a reference flat mirror that is substantially at a height of the wafer surface. For at least this reason, it would not have been obvious to modify the Kawashima apparatus to arrive at the apparatus as recited in claim 1.

Independent claim 5 is directed to a wafer edge exposure method including detecting the height of an edge of a semiconductor wafer, and controlling the focusing position of exposure light radiated toward the edge, on the basis of the height of the edge. Thus, for at least the same reasons as claim 1, claim 5 is also patentable over Kawashima.

The dependent claims ultimately depend from either claim 1 or claim 5 and are patentable for at least the same reasons, as well as for patentable features recited therein.

New claims 9 and 10, respectively depending from independent claims 1 and 5, have been added. Support for these new claims can be found in the present specification at least on page 6, lines 8-27. Claims 9 and 10 are patentable over Kawashima for at least the reasons given above with respect to claims 1 and 5.

For at least the reasons given above, applicant submits that the rejection under 35 U.S.C. 102 has been overcome, and respectfully request that the rejection be withdrawn.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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